CLAIMS

What is claimed is:

1. A multi-port packet switching device comprising:

a plurality of port units communicatively coupled in a packet transport time division multiplexed (TDM) configuration, the packet TDM configuration transporting a packet in one or more cells of about equal size, the one or more cells including a start cell including an internal header; and

each of the port units being communicatively coupled to an address lookup module and an external device interface, the address lookup module comprising logic for determining a multi-bit destination queue map for the packet, the multi-bit destination queue map including a group of bits for each port unit and each group of bits including at least one bit for each queue in each port unit. .

2. The multi-port packet switching device of claim 1 wherein each port unit comprises:

a packet transport TDM controller for receiving the start cell from the packet TDM configuration and determining if its port is the packet destination for the packet based on the multi-bit destination queue map for the packet;

a transmit buffer communicatively coupled to the packet transport TDM controller for receiving one or more cells of a packet destined for its port, the transmit buffer comprising a plurality of queues; a transmit buffer manager for controlling storage of the one or more cells in the transmit buffer wherein the transmit buffer manager maintains a context of memory space for each of the other packet sources of the packet transport TDM configuration from which a packet is being stored;

the transmit buffer manager maintaining a write pointer for each of the other packet sources in the configuration;

a receive buffer for receiving one or more cells of an ingress packet;

an external device interface for sending the ingress packet to the receive buffer; and

a lookup controller for extracting search parameters from a header of the ingress packet, the lookup controller being communicatively coupled to the address lookup module, the address lookup module determining the destination queue map for the packet based on the search parameters.

3. The multi-port packet switching device of claim 1 wherein the configuration is a ring configuration.

4. The multi-port packet switching device of claim 1 wherein the configuration is a linear chain configuration.

5. The switching device of claim 2 wherein the one or more cells of each packet stored in each context are stored contiguously.

6. The switching device of claim 1 wherein the switching device is an Ethernet switching device.

7. The switching device of claim 1 wherein the switching device is implemented as a single chip.

8. The switching device of claim 4 wherein the switching device is an Ethernet switching device implemented as a single chip wherein the external device interface is an Ethernet media access controller (MAC) having a speed of at least about 10 Gbps.

9. In a multi-port packet switching device comprising a plurality of port units communicatively coupled in a packet transport time division multiplexed (TDM) configuration, the packet TDM configuration transporting a packet in one or more cells of about equal size, the cells including a first cell including a packet header of the packet, the method comprising:

determining a multi-bit queue map for a packet to be sent to the packet TDM configuration wherein the multi-bit queue map includes a group of bits for each port unit in the configuration and each group of bits including at least one bit for each queue in each port unit, wherein the controller accesses the group of bits for its port unit and determines based on the queue bits if the one or more cells of the packet are destined for its port unit;

prepending the queue map as an internal header in the first cell of the packet; and

transmitting the one or more cells of the packet onto the packet TDM configuration.

10. The method of claim 9 further comprising:

receiving the first cell of a packet including the multi-bit queue map;

determining the destination queue in a transmit buffer of the port unit based on the multi-bit queue map;

allocating sufficient storage space for the packet in a context of memory space associated with the packet source of the packet in the destination queue based on a size of the packet indicated in the header of the first cell; and

storing one or more cells of the packet contiguously in the context of memory space.